

TITLE OF THE INVENTION

SYMMETRICAL CLOCK DISTRIBUTION IN MULTI-STAGE HIGH SPEED DATA
CONVERSION CIRCUITS

ABSTRACT OF THE DISCLOSURE

5 The present invention provides a high speed bit stream data conversion circuit that includes input ports to receive first bit streams at a first bit rate. Data conversion circuits receive the first bit streams and produce second bit stream(s), wherein the number and bit
10 rate of the first and second bit stream(s) differ. Symmetrical pathways transport the first bit streams from the input ports to the data conversion circuits, wherein their transmission time(s) are substantially equal. A clock distribution circuit receives and symmetrically distributes a clock signal to data conversion circuits. A central trunk coupled to the clock port and located between a first pair of circuit pathways with paired branches that extend
15 from the trunk and that couple to the data conversion circuits make up the clock distribution circuit. The distributed data clock signal latches data in data conversion circuits from the first to the second bit stream(s).